data read out from said memory based on an indication from said processor.

~~17~~ 25. A memory controller according to claim ~~16~~ 24, wherein said successive groups of m bits of data from said m bit terminals are read out of said memory by performing plural read operations within a memory cycle based on an address specified by said processor.

~~18~~ 26. A memory controller according to claim ~~17~~ 25, wherein said n bits of data is applied to said processor through said n bit terminals in a unit of time more than two times said memory cycle.

~~19~~ 27. A memory controller according to claim ~~16~~ 24, wherein said successive groups of m bits of data each includes an m bit portion of said n bits of data.

REMARKS

Entry of the above amendments is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees,

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Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 312-6600